Synopsys Timing Constraints And Optimization

10th International Workshop, PATMOS 2000, Göttingen, Germany, September 13-15, 2000 Proceedings
Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation
A Practical Guide to Synopsys Design Constraints (SDC)
Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation
EDA for IC Implementation, Circuit Design, and Process Technology
Timing Analysis and Optimization of Sequential Circuits
A Practical Approach
12th International Workshop, PATMOS 2002, Seville, Spain, September 11 - 13, 2002
20th International Workshop, PATMOS 2010, Grenoble, France, September 7-10, 2010, Revised Selected Papers
Closing the Gap Between ASIC & Custom
Static Timing Analysis for Nanometer Designs
Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation
Energy Optimization and Scavenging Techniques
Integrated Circuit and System Design: Power and Timing Modeling, Optimization and Simulation
Best Practices for Team-based Design
Design for High Performance, Low Power, and Reliable 3D Integrated Circuits
21st International Workshop, PATMOS 2011, Madrid, Spain, September 26-29, 2011, Proceedings
Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology
22nd International Workshop, PATMOS 2012, Newcastle upon Tyne, UK, September 4-6, 2012, Revised Selected Papers
Logic Synthesis and SOC Prototyping
FPGA Design
Statistical Analysis and Optimization for VLSI: Timing and Power
Integrated Circuit and System Design. Power and Timing Modeling, Optimization, and Simulation
The Art of Timing Closure
RTL Design using VHDL
Integrated Circuit Design. Power and Timing Modeling, Optimization and Simulation
Advanced ASIC Design Implementation
Logic Synthesis Using Synopsys®
Logic and Architecture Synthesis
Using Synopsys® Design CompilerTM and PrimeTime®
Best Practices for Team-based Reuse
Tools and Techniques for High-Performance ASIC Design
Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation
Leakage Power Analysis and Optimization in Deep-Submicron Technologies Under Process Variation
FPGA Design
Advanced ASIC Chip Synthesis
16th International Workshop, PATMOS 2006, Montpellier, France, September 13-15, 2006, Proceedings
15th International Workshop, PATMOS 2005, Leuven, Belgium, September 21-23, 2005, Proceedings
Digitally-Assisted Analog and Analog-Assisted Digital IC Design

ACEVEDO SANTANA

10th International Workshop, PATMOS 2000, Göttingen, Germany, September 13-15, 2000 Proceedings Springer Science & Business Media
Adoption and Optimization of Embedded and Real-Time Communication Systems presents innovative research on the integration of embedded systems, real-time systems and the developments towards multimedia technology. This book is essential for researchers, practitioners, scientists, and IT professionals interested in expanding their knowledge of this interdisciplinary field.
Springer Science & Business Media
Welcome to the proceedings of PATMOS 2008, the 18th in a series of int- national workshops. PATMOS 2008 was organized by INESC-ID / IST - TU Lisbon, Portugal, with sponsorship by Cadence, IBM, Chipidea, and Tecmic, and technical co-sponsorship by the IEEE. Over the years, PATMOS has evolved into an important European event, where researchers from both industry and academia discuss and investigate the emerging challenges in future and contemporary applications, design methodologies, and tools required for the development of the upcoming generations of integrated circuits and systems. The technical program of PATMOS 2008 c- tained state-of-the-art technical contributions, three invited talks, and a special session on recon?gurable architectures. The technical program focused on t- ing, performance and power consumption, as well as architectural aspects with particular emphasis on modeling, design, characterization, analysis and op- mization in the nanometer era. The Technical Program Committee, with the assistance of additional expert reviewers, selected the 41 papers presented at PATMOS. The papers were - ganized into 7 oral sessions (with a total of 31 papers) and 2 poster sessions (with a total of 10 papers). As is customary for the PATMOS workshops, full papers were required for review, and a minimum of three reviews were received per manuscript.
Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Springer Science & Business Media
This book describes best practices for successful FPGA design. It is the result of the author’s meetings with hundreds of customers on the challenges facing each of their FPGA design teams. By

gaining an understanding into their design environments, processes, what works and what does not work, key areas of concern in implementing system designs have been identified and a recommended design methodology to overcome these challenges has been developed. This book's content has a strong focus on design teams that are spread across sites. The goal being to increase the productivity of FPGA design teams by establishing a common methodology across design teams; enabling the exchange of design blocks across teams. Coverage includes the complete FPGA design flow, from the basics to advanced techniques. This new edition has been enhanced to include new sections on System modeling, embedded design and high level design. The original sections on Design Environment, RTL design and timing closure have all been expanded to include more up to date techniques as well as providing more extensive scripts and RTL code that can be reused by readers. Presents complete, field-tested methodology for FPGA design, focused on reuse across design teams; Offers best practices for FPGA timing closure, in-system debug, and board design; Details techniques to resolve common pitfalls in designing with FPGAs.

A Practical Guide to Synopsys Design Constraints (SDC) Springer Science & Business Media

This book serves as a hands-on guide to timing constraints in integrated circuit design. Readers will learn to maximize performance of their IC designs, by specifying timing requirements correctly. Coverage includes key aspects of the design flow impacted by timing constraints, including synthesis, static timing analysis and placement and routing. Concepts needed for specifying timing requirements are explained in detail and then applied to specific stages in the design flow, all within the context of Synopsys Design Constraints (SDC), the industry-leading format for specifying constraints.

Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Springer

Welcome to the proceedings of PATMOS 2003. This was the 13th in a series of international workshops held in several locations in Europe. Over the years, PATMOS has gained recognition as one of the major European events devoted to power and timing aspects of integrated circuit and system design. Despite its signi?cant growth and development, PATMOS can still be considered as a very informal forum, featuring high-level scienti?c presentations together with open discussions and panel sessions in a free and relaxed environment. This year, PATMOS took place in Turin, Italy, organized by the Politecnico di Torino, with technical co-sponsorship from the IEEE Circuits and Systems Society and the generous support of the European Commission, as well as that of several industrial sponsors, including BullDAST, Cadence, Mentor Graphics, STMicroelectronics, and Synopsys. The objective of the PATMOS workshop is to provide a forum to discuss and investigate the emerging problems in methodologies and tools for the design of new generations of integrated circuits and systems. A major emphasis of the technical program is on speed and low-power aspects, with particular regard to modeling, characterization, design, and architectures.

EDA for IC Implementation, Circuit Design, and Process Technology Springer Science & Business Media

This book constitutes the refereed proceedings of the 16th International Workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS 2006. The book presents 41 revised full papers and 23 revised poster papers together with 4 key notes and 3 industrial abstracts. Topical sections include high-level design, power estimation and modeling memory and register files, low-power digital circuits, busses and interconnects, low-power techniques, applications and SoC design, modeling, and more.

Timing Analysis and Optimization of Sequential Circuits Springer Science & Business Media

Recent years have seen rapid strides in the level of sophistication of VLSI circuits. On the performance front, there is a vital need for techniques to design fast, low-power chips with minimum area for increasingly complex systems, while on the economic side there is the vastly increased pressure of time-to-market. These pressures have made the use of CAD tools mandatory in designing complex systems. Timing Analysis and Optimization of Sequential Circuits describes CAD algorithms for analyzing and optimizing the timing behavior of sequential circuits with special reference to performance parameters such as power and area. A unified approach to performance analysis and optimization of sequential circuits is presented. The state of the art in timing analysis and optimization techniques is described for circuits using edge-triggered or level-sensitive memory elements. Specific emphasis is placed on two methods that are true sequential timing optimizations techniques: retiming and clock skew optimization. Timing Analysis and Optimization of Sequential Circuits covers the following topics: Algorithms for sequential timing analysis Fast algorithms for clock skew optimization and their applications Efficient techniques for retiming large sequential circuits Coupling sequential and combinational optimizations. Timing Analysis and Optimization of Sequential Circuits is written for graduate students, researchers and professionals in the area of CAD for VLSI and VLSI circuit design.

A Practical Approach Springer Nature

Presenting a comprehensive overview of the design automation algorithms, tools, and methodologies used to design integrated circuits, the Electronic Design Automation for Integrated Circuits Handbook is available in two volumes. The second volume, EDA for IC Implementation, Circuit Design, and Process Technology, thoroughly examines real-time logic to GDSII (a file format used to transfer data of semiconductor physical layout), analog/mixed signal design, physical verification, and technology CAD (TCAD). Chapters contributed by leading experts authoritatively discuss design for manufacturability at the nanoscale, power supply network design and analysis, design modeling, and much more. Save on the complete set.

12th International Workshop, PATMOS 2002, Seville, Spain, September 11 - 13, 2002 Springer Science & Business Media

This book provides a comprehensive overview of key technologies being used to address challenges raised by continued device scaling and the extending gap between memory and central processing unit performance. Authors discuss in detail what are known commonly as "More than Moore" (MtM), technologies, which add value to devices by incorporating functionalities that do not necessarily scale according to "Moore's Law". Coverage focuses on three key technologies needed for efficient power management and cost per performance: novel memories, 3D integration and photonic on-chip interconnect.

20th International Workshop, PATMOS 2010, Grenoble, France, September 7-10, 2010, Revised Selected Papers Springer

In August of 2006, an engineering VP from one of Altera's customers approached Misha Burich, VP of Engineering at Altera, asking for help in reliably being able to predict the cost, schedule and quality of system designs reliant on FPGA designs. At this time, I was responsible for defining the design flow requirements for the Altera design software and was tasked with investigating this further. As I worked with the customer to understand what worked and what did not work reliably in their FPGA design process, I noted that this problem was not unique to this one customer. The characteristics of the problem are shared by many

Corporations that implement designs in FPGAs. The Corporation has many design teams at different locations and the success of the FPGA projects vary between the teams. There is a wide range of design experience across the teams. There is no working process for sharing design blocks between engineering teams. As I analyzed the data that I had received from hundreds of customer visits in the past, I noticed that design reuse among engineering teams was a challenge. I also noticed that many of the design teams at the same Companies and even within the same design team used different design methodologies. Altera had recently solved this problem as part of its own FPGA design software and IP development process.

Closing the Gap Between ASIC & Custom Elsevier

Logic synthesis has become a fundamental component of the ASIC design flow, and Logic Synthesis Using Synopsys® has been written for all those who dislike reading manuals but who still like to learn logic synthesis as practised in the real world. The primary focus of the book is Synopsys Design Compiler®: the leading synthesis tool in the EDA marketplace. The book is specially organized to assist designers accustomed to schematic capture based design to develop the required expertise to effectively use the Compiler. Over 100 `classic scenarios' faced by designers using the Design Compiler have been captured and discussed, and solutions provided. The scenarios are based both on personal experiences and actual user queries. A general understanding of the problem-solving techniques provided will help the reader debug similar and more complicated problems. Furthermore, several examples and dc-shell scripts are provided. Specifically, Logic Synthesis Using Synopsys® will help the reader develop a better understanding of the synthesis design flow, optimization strategies using the Design Compiler, test insertion using the Test Compiler®, commonly used interface formats such as EDIF and SDF, and design re-use in a synthesis-based design methodology. Examples have been provided in both VHDL and Verilog. Audience: Written with CAD engineers in mind to enable them to formulate an effective synthesis-based ASIC design methodology. Will also assist design teams to better incorporate and effectively integrate synthesis with their existing in-house design methodology and CAD tools.

Static Timing Analysis for Nanometer Designs Springer

A practical guide to help electronics designers and students make the most of VHDL with the latest, most widely-used design tools available.This book presents both the professional and academic side of designing with VHDL, and shows how to take full advantage of VHDL with today's design tools. It contains many worked examples developed with Synopsys, Mentor Graphics and ViewLook tools. It reviews concurrent, sequential and structural VHDL, RAM and ROM development, state machines, and RTL synthesis. Test methodologies and rapid prototyping are covered, as well as examples of quality design and common errors to avoid. End-of-chapter exercises and laboratories are included throughout.For both engineering professionals and students interested in using VHDL as effectively as possible in their environments.

Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation CRC Press

This book constitutes the refereed proceedings of the 10th International Workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS 2000, held in GÃ¶ttingen, Germany in September 2000. The 33 revised full papers presented were carefully reviewed and selected for inclusion in the book. The papers are organized in sections on RTL power modeling, power estimation and optimization, system-level design, transistor level design, asynchronous circuit design, power efficient technologies, design of multimedia processing applications, adiabatic design and arithmetic modules, and analog-digital circuit modeling.

Energy Optimization and Scavenging Techniques Springer

Advanced ASIC Chip Synthesis: Using Synopsys® Design Compiler® and PrimeTime® describes the advanced concepts and techniques used for ASIC chip synthesis, formal verification and static timing analysis, using the Synopsys suite of tools. In addition, the entire ASIC design flow methodology targeted for VDSM (Very-Deep-Sub-Micron) technologies is covered in detail. The emphasis of this book is on real-time application of Synopsys tools used to combat various problems seen at VDSM geometries. Readers will be exposed to an effective design methodology for handling complex, sub-micron ASIC designs. Significance is placed on HDL coding styles, synthesis and optimization, dynamic simulation, formal verification, DFT scan insertion, links to layout, and static timing analysis. At each step, problems related to each phase of the design flow are identified, with solutions and work-arounds described in detail. In addition, crucial issues related to layout, which includes clock tree synthesis and back-end integration (links to layout) are also discussed at length. Furthermore, the book contains in-depth discussions on the basics of Synopsys technology libraries and HDL coding styles, targeted towards optimal synthesis solutions. Advanced ASIC Chip Synthesis: Using Synopsys® Design Compiler® and PrimeTime® is intended for anyone who is involved in the ASIC design methodology, starting from RTL synthesis to final tape-out. Target audiences for this book are practicing ASIC design engineers and graduate students undertaking advanced courses in ASIC chip design and DFT techniques. From the Foreword: `This book, written by Himanshu Bhatnagar, provides a comprehensive overview of the ASIC design flow targeted for VDSM technologies using the Synopsis suite of tools. It emphasizes the practical issues faced by the semiconductor design engineer in terms of synthesis and the integration of front-end and back-end tools. Traditional design methodologies are challenged and unique solutions are offered to help define the next generation of ASIC design flows. The author provides numerous practical examples derived from real-world situations that will prove valuable to practicing ASIC design engineers as well as to students of advanced VLSI courses in ASIC design'. Dr Dwight W. Decker, Chairman and CEO, Conexant Systems, Inc., (Formerly, Rockwell Semiconductor Systems), Newport Beach, CA, USA.

Integrated Circuit and System Design: Power and Timing Modeling, Optimization and Simulation Springer Science & Business Media

Constraining Designs for Synthesis and Timing AnalysisA Practical Guide to Synopsys Design Constraints (SDC)Springer Science & Business Media

Best Practices for Team-based Design John Wiley & Sons

iming, timing, timing! That is the main concern of a digital designer charged with designing a semiconductor chip. What is it, how is it T described, and how does one verify it? The design team of a large digital design may spend months architecting and iterating the design to achieve the required timing target. Besides functional verification, the t- ing closure is the major milestone which dictates when a chip can be - leased to the semiconductor foundry for fabrication. This book addresses the timing verification using static timing analysis for nanometer designs. The book has originated from many years of our working in the area of timing verification for complex nanometer designs. We have come across many design engineers trying to learn the background and various aspects of static timing analysis. Unfortunately, there is no book currently ava- able that can be used by a working engineer to get acquainted with the - tails of

static timing analysis. The chip designers lack a central reference for information on timing, that covers the basics to the advanced timing veri- cation procedures and techniques.

Design for High Performance, Low Power, and Reliable 3D Integrated Circuits Springer

The microelectronics market, with special emphasis to the production of complex mixed-signal systems-on-chip (SoC), is driven by three main dynamics, time-- market, productivity and managing complexity. Pushed by the progress in na- meter technology, the design teams are facing a curve of complexity that grows exponentially, thereby slowing down the productivity design rate. Analog design automation tools are not developing at the same pace of technology, once custom design, characterized by decisions taken at each step of the analog design flow, - lies most of the time on designer knowledge and expertise. Actually, the use of - sign management platforms, like the Cadences Virtuoso platform, with a set of - tegrated CAD tools and database facilities to deal with the design transformations from the system level to the physical implementation, can significantly speed-up the design process and enhance the productivity of analog/mixed-signal integrated circuit (IC) design teams. These design management platforms are a valuable help in analog IC design but they are still far behind the development stage of design automation tools already available for digital design. Therefore, the development of new CAD tools and design methodologies for analog and mixed-signal ICs is ess- tial to increase the designer’s productivity and reduce design productivitygap. The work presented in this book describes a new design automation approach to the problem of sizing analog ICs.

21st International Workshop, PATMOS 2011, Madrid, Spain, September 26-29, 2011, Proceedings Springer Nature

The second of two volumes in the Electronic Design Automation for Integrated Circuits Handbook, Second Edition, Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology thoroughly examines real-time logic (RTL) to GDSII (a file format used to transfer data of semiconductor physical layout) design flow, analog/mixed signal design, physical verification, and technology computer-aided design (TCAD). Chapters contributed by leading experts authoritatively discuss design for manufacturability (DFM) at the nanoscale, power supply network design and analysis, design modeling, and much more. New to This Edition: Major updates appearing in the initial phases of the design flow, where the level of abstraction keeps rising to support more functionality with lower non-recurring engineering (NRE) costs Significant revisions reflected in the final phases of the design flow, where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting-edge applications and approaches realized in the decade since publication of the previous edition—these are illustrated by new chapters on 3D circuit integration and clock design Offering improved depth and modernity, Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology provides a valuable, state-of-the-art reference for electronic design automation (EDA) students, researchers, and professionals.

Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology Constraining Designs for Synthesis and Timing AnalysisA Practical Guide to Synopsys Design Constraints (SDC)

Advanced ASIC Chip Synthesis: Using Synopsys® Design Compiler® Physical Compiler® and PrimeTime®, Second Edition describes the advanced concepts and techniques used towards ASIC chip synthesis, physical synthesis, formal verification and static timing analysis, using the Synopsys suite of tools. In addition, the entire ASIC design flow methodology targeted for VDSM (Very-Deep-Sub-Micron) technologies is covered in detail. The emphasis of this book is on real-time application of Synopsys tools, used to combat various problems seen at VDSM geometries. Readers will be exposed to an effective design methodology for handling complex, sub-micron ASIC designs. Significance is placed on HDL coding styles, synthesis and optimization, dynamic simulation, formal verification, DFT scan insertion, links to layout, physical synthesis, and static timing analysis. At each step, problems related to each phase of the design flow are identified, with solutions and work-around described in detail. In addition, crucial issues related to layout, which includes clock tree synthesis and back-end integration (links to layout) are also discussed at length. Furthermore, the book contains in-depth discussions on the basis of Synopsys technology libraries and HDL coding styles, targeted towards optimal synthesis solution. Target audiences for this book are practicing ASIC design engineers and masters level students undertaking advanced VLSI courses on ASIC chip design and DFT techniques.

22nd International Workshop, PATMOS 2012, Newcastle upon Tyne, UK, September 4-6, 2012, Revised Selected Papers Springer Science & Business Media

th Welcome to the proceedings of PATMOS 2007, the 17 in a series of international workshops. PATMOS 2007 was organized by Chalmers University of Technology with IEEE Sweden Chapter of the Solid-State Circuit Society technical - sponsorship and IEEE CEDA sponsorship. Over the years, PATMOS has evolved into an important European event, where - searchers from both industry and academia discuss and investigate the emerging ch- lenges in future and contemporary applications, design methodologies, and tools - quired for the development of the upcoming generations of integrated circuits and systems. The technical program of PATMOS 2007 consisted of state-of-the-art te- nical contributions, three invited talks and an industrial session on design challenges in real-life projects. The technical program focused on timing, performance and power consumption, as well as architectural aspects with particular emphasis on m- eling, design, characterization, analysis and optimization in the nanometer era. The Technical Program Committee, with the assistance of additional expert - viewers, selected the 55 papers presented at PATMOS. The papers were organized into 9 technical sessions and 3 poster sessions. As is always the case with the PATMOS workshops, full papers were required, and several reviews were received per manuscript.