
Zynq Ultrascale Mpsoc For The System Architect Logtel

Zynq UltraScale+ MPSoC ZCU102 Evaluation Kit

ZynQ ultrascale+ MPSoC SOM | ZU7/5/4 ZynQ UI+ MPSoC ...

Zynq Ultrascale Mpsoc For The

Zynq® UltraScale+™ MPSoC for the System Architect

Zynq UltraScale+ MPSoC Processing System v3

Zynq Ultrascale+MPSoC IP Overview on VIVADO (APU, RPU \u0026amp; GPU

Configuration) Single Chip 4K Video Processing with Zynq UltraScale+ MPSoC Setting

up the ZCU104 Zynq Ultrascale+ to run PYNQ Root Port Made Simple for Zynq

UltraScale+ Zynq Ultrascale+ and Petalinux - part 1 - introduction \$599 Xilinx ZYNQ

UltraScale MPSoC VECP Kit with MIPI-CSI for image processing Xilinx Zynq®

UltraScale+ MPSoC Multiprocessors | Featured Product Spotlight Xilinx Zynq®

UltraScale+™ MPSoC ZCU102 Evaluation Kit | New Product Brief Zynq UltraScale+

MPSoC development flow using the SDSoC Development Environment Ultra96 Xilinx

Zynq UltraScale+ MPSoC Development Board UltraScale ASIC-like clocking Real-time

Video Processing on Zybo FPGA Zybo Z7 Introduction

First FPGA experiences with a Digilent Cora Z7 Xilinx Zynq ~~Introduction to QEMU XEN for Real-Time Interference-Free Virtualization with Zynq® UltraScale+™ MPSoC Hello Ultra96! Getting Started with the Ultimate SoC Board FPGA YOLOv2 on the Xilinx ZCU102 Zynq UltraScale+ MPSoC Board Python on Zynq FPGA for Convolutional Neural Networks (Xilinx XOHW17 XIL 11000)~~ **Booting Linux on the Xilinx ZCU111 board using the 2018.3 PetaLinux BSP's pre-built images** ~~Andromium OS on MHL Lapdock, Productivity multi-window UI for Android What is ZYNQ? (Lesson 1) Vivado PS Configuration Wizard Overview 4K Video Conferencing with Zynq UltraScale+ MPSoC Zynq UltraScale+ says, "Hello World!"~~ **Embedded Vision and Control Solutions with the Zynq UltraScale+ MPSoC Video-14: UG1209 : Zynq UltraScale+ MPSoC : Embedded Design - QSPI Book Mode ZCU102 Avnet shows \$249 Ultra96 Xilinx Zynq UltraScale+ MPSoC development board**

Zynq UltraScale+ MPSoC - Xilinx

Zynq MPSoC Book - With PNYQ and Machine Learning Applications

Solved: ZYNQ UltraScale+ MPSoC with 16-bit width DDR4 prob ...

Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching ...

Xilinx Customer Learning Center

Zynq® UltraScale+™ MPSoC for the Software Developer | BLT

Development kit | zu19/17/11 zynq ultrascale+ mpsoC ...
Zynq UltraScale+ MPSoC Datasheet - Xilinx | DigiKey
Zynq UltraScale+ MPSoC Base Targeted Reference Design
Zynq UltraScale+ MPSoCs Multiprocessors - Xilinx | Mouser
UltraScale MPSoC Architecture - Xilinx
Automotive Grade Zynq UltraScale+ MPSoCs
Zynq UltraScale+ MPSoC Data Sheet: Overview (DS891)

*Zynq Ultrascale Mpsoc
For The System
Architect Logtel*

*Downloaded from
<ftp.wtvq.com> by guest*

KENNEDY KENNEDI

**Zynq UltraScale+ MPSoC ZCU102
Evaluation Kit** *Zynq Ultrascale+MPSoC
IP Overview on VIVADO (APU, RPU
|u0026 GPU Configuration) Single-Chip
4K Video Processing with Zynq
UltraScale+ MPSoC Setting up the
ZCU104 Zynq Ultrascale+ to run PYNQ
Root-Port Made Simple for Zynq*

*UltraScale+ Zynq Ultrascale+ and
Petalinux - part 1 - introduction \$599
Xilinx ZYNQ UltraScale MPSoC VECP Kit
with MIPI-CSI for image processing Xilinx
Zynq® UltraScale+ MPSoC
Multiprocessors | Featured Product
Spotlight Xilinx Zynq® UltraScale+™
MPSoC ZCU102 Evaluation Kit | New
Product Brief Zynq UltraScale+ MPSoC
development flow using the SDSoC
Development Environment Ultra96 Xilinx
Zynq UltraScale+ MPSoC Development*

~~Board UltraScale ASIC-like clocking Real-time Video Processing on Zybo FPGA Zybo Z7 Introduction~~

First FPGA experiences with a Digilent Cora Z7 Xilinx Zynq Introduction to QEMU XEN for Real-Time Interference-Free Virtualization with Zynq® UltraScale+™ MPSoC Hello Ultra96! Getting Started with the Ultimate SoC Board FPGA YOLOv2 on the Xilinx ZCU102 Zynq UltraScale+ MPSoC Board Python on Zynq FPGA for Convolutional Neural Networks (Xilinx XOHW17 XIL-11000) **Booting Linux on the Xilinx ZCU111 board using the 2018.3 PetaLinux BSP's pre-built images** Andromium OS on MHL Lapdock, Productivity multi-window UI for Android *What is ZYNQ? (Lesson 1)*

Vivado PS Configuration Wizard Overview 4K Video Conferencing with Zynq UltraScale+ MPSoC Zynq UltraScale+ says, "Hello World!"

Embedded Vision and Control Solutions with the Zynq UltraScale+ MPSoC Video-14: UG1209 : Zynq UltraScale+ MPSoC : Embedded Design - QSPI Book Mode ZCU102 Avnet shows \$249 Ultra96 Xilinx Zynq UltraScale+ MPSoC development board Zynq Ultrascale Mpsoc For TheZynq® UltraScale+™ MPSoC devices provide 64-bit processor scalability while combining real-time control with soft and hard engines for graphics, video, waveform, and packet processing. Zynq UltraScale+ MPSoC - XilinxThe Xilinx Automotive XA Zynq® UltraScale+™ MPSoC family is qualified

according to AEC-Q100 test specifications with full ISO26262 ASIL-C level certification. The product integrates a feature-rich 64-bit quad-core ARM® Cortex™ -A53 and dual-core ARM Cortex-R5 based processing system (PS) and Xilinx programmable logic (PL) UltraScale architecture in a single device. Automotive Grade Zynq UltraScale+ MPSoCs Zynq® UltraScale+™ MPSoC for the Software Developer. This two-day course is structured to provide software developers with a catalog of OS implementation options, including hypervisors, various Linux implementations, booting and configuring a system, and power management for the Zynq® UltraScale+™ MPSoC family.. Skills Gained Zynq® UltraScale+™ MPSoC for

the Software Developer | BLT The UltraScale™ MPSoC Architecture is built on TSMC's 16FinFET+ process technology and enables next-generation Zynq® UltraScale+ MPSoCs. Building on the industry success of the Zynq-7000 SoC family, the new UltraScale MPSoC architecture extends Xilinx SoCs to enable true heterogeneous multi-processing with 'the right engines for the right tasks' for smarter systems, including: UltraScale MPSoC Architecture - Xilinx View Zynq UltraScale+ MPSoC Datasheet from Xilinx Inc. at Digikey ... the B2104 packages are compatible with Virtex UltraScale+ devices and Kintex UltraScale devices in the . B2104 packages. All valid device/package combinations are provided in the Device-Package Combinations . Zynq

UltraScale+ MPSoC Datasheet - Xilinx | DigiKey
 The Zynq® UltraScale+™ MPSoC Processing System wrapper instantiates the processing system section of the Zynq UltraScale+ MPSoC for the programmable logic and external board logic. The wrapper includes unaltered connectivity and some logic functions for some signals.
 Zynq UltraScale+ MPSoC Processing System v3
 Xilinx Zynq® UltraScale+ MPSoCs Multiprocessors feature 64-bit processor scalability that combines real-time control with soft and hard engines for graphics, video, waveform, and packet processing. The multiprocessor systems-on-chip devices are built on a common real-time processor and programmable logic-equipped platform.
 Zynq UltraScale+ MPSoCs Multiprocessors - Xilinx |

Mouser
 The Xilinx® Zynq® UltraScale+™ MPSoCs are available in -3, -2, -1 speed grades, with -3E devices having the highest performance. The -2LE and -1LI devices can operate at a VCCINT voltage at 0.85V or 0.72V and are screened for lower maximum static power.
 Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching ...
 The Zynq® UltraScale+™ MPSoC family is based on the Xilinx® UltraScale™ MPSoC architecture. This family of products integrates a feature-rich 64-bit quad-core or dual-core Arm® Cortex™ -A53 and dual-core Arm Cortex-R5 based processing system (PS) and Xilinx programmable logic (PL) UltraScale architecture in a single device.
 Zynq UltraScale+ MPSoC Data Sheet: Overview (DS891)
 Zynq® UltraScale+™

MPSoC HW-SW Virtualization Covers the hardware and software elements of virtualization. The lab demonstrate how hypervisors can be used. QEMU Introduction to the Quick Emulator, which is the tool used to run software for the Zynq® UltraScale+™ MPSoC device when hardware is not available. Zynq® UltraScale+™ MPSoC for the System Architect This kit features a Zynq® UltraScale+™ MPSoC with a quad-core Arm® Cortex®-A53, dual-core Cortex-R5F real-time processors, and a Mali™-400 MP2 graphics processing unit based on Xilinx's 16nm FinFET+ programmable logic fabric. The ZCU102 supports all major peripherals and interfaces, enabling development for a wide range of applications. Zynq UltraScale+ MPSoC ZCU102 Evaluation

Kit The Zynq® UltraScale+™ MPSoC base targeted reference design (TRD) is an embedded video processing application that is partitioned between the SoC's processing system (PS) and programmable logic (PL) for optimal performance. Zynq UltraScale+ MPSoC Base Targeted Reference Design Zynq UltraScale+ MPSoC for the Hardware Designer. Add to Cart. USD Price = 199; Training Credit Price = 2 TC Show Detailed Course Description. Overview. This course provides hardware designers with an overview of the capabilities and support for the Zynq® UltraScale+™ MPSoC family from a hardware architectural perspective. ... Xilinx Customer Learning Center From vivado 2019.1, zynq mpsoc PS support 16-bit width DDR4 memory interface, we

verified this configuration in ZCU102 and ZCU104, they work well. So we design our board use mp soc with one x16 DDR4 component, but it work abnormal, ps boot failed. After a hard time of hardware debugging, we didn't find anything wrong in our design. Solved: ZYNQ Ultrascale+ MPSOC with 16-bit width DDR4 prob ... This book introduces the Zynq® MPSoC (Multi-Processor System-on-Chip), an embedded device from Xilinx® that combines a processing system that includes Arm® Cortex®-A53 application and Arm Cortex-R5 real-time processors, alongside FPGA programmable logic. Zynq MPSoc Book - With PNYQ and Machine Learning Applications The MPSoC supports Quad/Dual Cortex A53 up to 1.5GHz with programmable logic cells ranging from

192K to 504K. The SOM supports high-speed connectivity peripherals such as PCIe, USB3.0, SATA3.1, Display port, Gigabit Ethernet through GTR high-speed transceivers from MPSoC. Mouse over the image for zoom ZynQ ultrascale+ MPSoC SOM | ZU7/5/4 ZynQ UI+ MPSoC ... The Zynq Ultrascale+ MPSoC development kit carrier board supports the required set of features like FMC+ (HPC), FMC (HPC), FireFly, QSFP, SFP+, 12-Pin Pmod, and HDMI- IN/OUT connectors to validate Zynq Ultrascale+ MPSoC high-speed PL interfaces and PCIe x4, SATA, USB-Type-C, Display Port, Gigabit Ethernet and SDI Video IN/OUT on-board connectors to validate the Zynq Ultrascale+ MPSoC high-speed PS interfaces. Development kit | zu19/17/11 zynq ultrascale+ mp soc ... Zynq

UltraScale+ MPSoC Application

Processing Unit – Introduction to the members of the APU, specifically the Cortex™-A53 processor and how the cluster is configured and managed. Zynq UltraScale+ MPSoC HW-SW Virtualization – Covers the hardware and software elements of virtualization. The lab demonstrates how hypervisors can be used.

Zynq® UltraScale+™ MPSoC HW-SW Virtualization Covers the hardware and software elements of virtualization. The lab demonstrate how hypervisors can be used. QEMU Introduction to the Quick Emulator, which is the tool used to run software for the Zynq® UltraScale+™ MPSoC device when hardware is not available.

ZynQ ultrascale+ MPSoC SOM | ZU7/5/4

ZynQ UI+ MPSoC ...

This book introduces the Zynq® MPSoC (Multi-Processor System-on-Chip), an embedded device from Xilinx® that combines a processing system that includes Arm® Cortex®-A53 application and Arm Cortex-R5 real-time processors, alongside FPGA programmable logic.

Zynq Ultrascale Mpsoc For The

Zynq® UltraScale+™ MPSoC for the Software Developer. This two-day course is structured to provide software developers with a catalog of OS implementation options, including hypervisors, various Linux implementations, booting and configuring a system, and power management for the Zynq® UltraScale+™ MPSoC family.. Skills Gained

Zynq® UltraScale+™ MPSoC for the System Architect

From vivado 2019.1, zynq mpsoC PS support 16-bit width DDR4 memory interface, we verified this configuration in ZCU102 and ZCU104, they work well. So we design our board use mpsoC with one x16 DDR4 component, but it work abnormal, ps boot failed. After a hard time of hardware debugging, we didn't find anything wrong in our design.

Zynq UltraScale+ MPSoC Processing System v3

View Zynq UltraScale+ MPSoC Datasheet from Xilinx Inc. at Digikey ... the B2104 packages are compatible with Virtex UltraScale+ devices and Kintex UltraScale devices in the . B2104 packages. All valid device/package combinations are provided in the Device-Package

Combinations .

Zynq UltraScale+MPSoC IP Overview on VIVADO (APU, RPU \u0026amp; GPU Configuration) Single-Chip 4K-Video Processing with Zynq UltraScale+ MPSoC Setting-up the ZCU104 Zynq UltraScale+ to run PYNQ Root-Port Made Simple for Zynq UltraScale+ Zynq UltraScale+ and Petalinux - part 1 - introduction \$599 Xilinx ZYNQ UltraScale MPSoC VECP Kit with MIPI-CSI for image processing Xilinx Zynq® UltraScale+ MPSoC Multiprocessors | Featured Product Spotlight Xilinx Zynq® UltraScale+™ MPSoC ZCU102 Evaluation Kit | New Product Brief Zynq UltraScale+ MPSoC development flow using the SDSoC Development Environment Ultra96 Xilinx Zynq UltraScale+ MPSoC Development Board UltraScale ASIC-like clocking Real-

*time Video Processing on Zybo FPGA
Zybo Z7 Introduction*

*First FPGA experiences with a Digilent
Cora Z7 Xilinx Zynq Introduction to
QEMU XEN for Real-Time Interference-
Free Virtualization with Zynq®
UltraScale+™ MPSoC Hello Ultra96!
Getting Started with the Ultimate SoC
Board FPGA YOLOv2 on the Xilinx
ZCU102 Zynq Ultrascale+ MPSoC Board
Python on Zynq FPGA for Convolutional
Neural Networks (Xilinx XOHW17
XIL-11000) **Booting Linux on the
Xilinx ZCU111 board using the
2018.3 PetaLinux BSP's pre-built
images** Andromium OS on MHL
Lapdock, Productivity multi-window UI
for Android What is ZYNQ? (Lesson 1)
Vivado PS Configuration Wizard*

*Overview 4K Video Conferencing with
Zynq UltraScale+ MPSoC Zynq
UltraScale+ says, "Hello World!"*

**Embedded Vision and Control
Solutions with the Zynq UltraScale+
MPSoC Video-14: UG1209 : Zynq
UltraScale+ MPSoC : Embedded
Design - QSPI Book Mode ZCU102
Avnet shows \$249 Ultra96 Xilinx
Zynq UltraScale+ MPSoC
development board**

This kit features a Zynq® UltraScale+™ MPSoC with a quad-core Arm® Cortex®-A53, dual-core Cortex-R5F real-time processors, and a Mali™-400 MP2 graphics processing unit based on Xilinx's 16nm FinFET+ programmable logic fabric. The ZCU102 supports all major peripherals and interfaces, enabling development for a wide range

of applications.

Zynq UltraScale+ MPSoC - Xilinx

Zynq Ultrascale+MPSoC IP Overview on VIVADO (APU, RPU \u0026amp; GPU Configuration)

Single Chip 4K Video Processing with Zynq UltraScale+ MPSoC

Setting up the ZCU104 Zynq Ultrascale+ to run PYNQ Root Port Made Simple for Zynq UltraScale+ Zynq Ultrascale+ and Petalinux - part 1 - introduction \$599

Xilinx ZYNQ UltraScale MPSoC VECP Kit with MIPI-CSI for image processing Xilinx Zynq® UltraScale+ MPSoC Multiprocessors | Featured Product Spotlight Xilinx Zynq® UltraScale+™ MPSoC ZCU102 Evaluation Kit | New Product Brief Zynq UltraScale+ MPSoC development flow using the SDSoC Development Environment Ultra96 Xilinx Zynq UltraScale+ MPSoC Development

Xilinx ZYNQ UltraScale MPSoC VECP Kit with MIPI-CSI for image processing Xilinx Zynq® UltraScale+ MPSoC Multiprocessors | Featured Product Spotlight Xilinx Zynq® UltraScale+™ MPSoC ZCU102 Evaluation Kit | New Product Brief Zynq UltraScale+ MPSoC development flow using the SDSoC Development Environment Ultra96 Xilinx Zynq UltraScale+ MPSoC Development

Multiprocessors | Featured Product Spotlight Xilinx Zynq® UltraScale+™ MPSoC ZCU102 Evaluation Kit | New Product Brief Zynq UltraScale+ MPSoC development flow using the SDSoC Development Environment Ultra96 Xilinx Zynq UltraScale+ MPSoC Development

Spotlight Xilinx Zynq® UltraScale+™ MPSoC ZCU102 Evaluation Kit | New Product Brief Zynq UltraScale+ MPSoC development flow using the SDSoC Development Environment Ultra96 Xilinx Zynq UltraScale+ MPSoC Development

Product Brief Zynq UltraScale+ MPSoC development flow using the SDSoC Development Environment Ultra96 Xilinx Zynq UltraScale+ MPSoC Development

development flow using the SDSoC Development Environment Ultra96 Xilinx Zynq UltraScale+ MPSoC Development

Development Environment Ultra96 Xilinx Zynq UltraScale+ MPSoC Development

Ultra96 Xilinx Zynq UltraScale+ MPSoC Development

Zynq UltraScale+ MPSoC Development

Board UltraScale ASIC-like clocking Real-time Video Processing on Zybo FPGA Zybo Z7 Introduction

First FPGA experiences with a Digilent Cora Z7 Xilinx Zynq Introduction to QEMU XEN for Real-Time Interference-Free Virtualization with Zynq® UltraScale+™ MPSoC Hello Ultra96!

Getting Started with the Ultimate SoC Board FPGA YOLOv2 on the Xilinx ZCU102 Zynq Ultrascale+ MPSoC Board Python on Zynq FPGA for Convolutional Neural Networks (Xilinx XOHW17 XIL-11000) Booting Linux on the Xilinx ZCU111 board using the 2018.3 PetaLinux BSP's pre-built images Andromium OS on MHL Lapdock, Productivity multi-window UI for Android What is ZYNQ? (Lesson 1)

UltraScale+™ MPSoC Hello Ultra96!

Getting Started with the Ultimate SoC Board FPGA YOLOv2 on the Xilinx ZCU102 Zynq Ultrascale+ MPSoC Board Python on Zynq FPGA for Convolutional Neural Networks (Xilinx XOHW17 XIL-11000) Booting Linux on the Xilinx ZCU111 board using the 2018.3 PetaLinux BSP's pre-built images Andromium OS on MHL Lapdock, Productivity multi-window UI for Android What is ZYNQ? (Lesson 1)

ZCU102 Zynq Ultrascale+ MPSoC Board Python on Zynq FPGA for Convolutional Neural Networks (Xilinx XOHW17 XIL-11000) Booting Linux on the Xilinx ZCU111 board using the 2018.3 PetaLinux BSP's pre-built images Andromium OS on MHL Lapdock, Productivity multi-window UI for Android What is ZYNQ? (Lesson 1)

Bootling Linux on the Xilinx ZCU111 board using the 2018.3 PetaLinux BSP's pre-built images Andromium OS on MHL Lapdock, Productivity multi-window UI for Android What is ZYNQ? (Lesson 1)

Images Andromium OS on MHL Lapdock, Productivity multi-window UI for Android What is ZYNQ? (Lesson 1)

Lapdock, Productivity multi-window UI for Android What is ZYNQ? (Lesson 1)

for Android What is ZYNQ? (Lesson 1)

[Vivado PS Configuration Wizard Overview 4K Video Conferencing with Zynq UltraScale+ MPSoC Zynq UltraScale+ says, "Hello World!"](#)

Embedded Vision and Control Solutions with the Zynq UltraScale+ MPSoC Video-14: UG1209 : Zynq UltraScale+ MPSoC : Embedded Design - QSPI Book Mode ZCU102 Avnet shows \$249 Ultra96 Xilinx Zynq UltraScale+ MPSoC development board Zynq MPSoc Book - With PNYQ and Machine Learning Applications

The UltraScale™ MPSoC Architecture is built on TSMC's 16FinFET+ process technology and enables next-generation Zynq® UltraScale+ MPSoCs. Building on the industry success of the Zynq-7000 SoC family, the new UltraScale MPSoC

architecture extends Xilinx SoCs to enable true heterogeneous multi-processing with 'the right engines for the right tasks' for smarter systems, including:

[Solved: ZYNQ Ultrascale+ MPSOC with 16-bit width DDR4 prob ...](#)

The Xilinx® Zynq® UltraScale+™ MPSoCs are available in -3, -2, -1 speed grades, with -3E devices having the highest performance. The -2LE and -1LI devices can operate at a VCCINT voltage at 0.85V or 0.72V and are screened for lower maximum static power.

Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching ...

Xilinx Zynq® UltraScale+ MPSoCs Multiprocessors feature 64-bit processor scalability that combines real-time control with soft and hard engines for

graphics, video, waveform, and packet processing. The multiprocessor systems-on-chip devices are built on a common real-time processor and programmable logic-equipped platform.

Xilinx Customer Learning Center

The Zynq® UltraScale+™ MPSoC base targeted reference design (TRD) is an embedded video processing application that is partitioned between the SoC's processing system (PS) and programmable logic (PL) for optimal performance.

Zynq® UltraScale+™ MPSoC for the Software Developer | BLT

Zynq UltraScale+ MPSoC Application Processing Unit - Introduction to the members of the APU, specifically the Cortex™-A53 processor and how the cluster is configured and managed. Zynq

UltraScale+ MPSoC HW-SW Virtualization - Covers the hardware and software elements of virtualization. The lab demonstrates how hypervisors can be used.

Development kit | zu19/17/11 zynq ultrascale+ mpsoc ...

Zynq UltraScale+ MPSoC for the Hardware Designer. Add to Cart. USD Price = 199; Training Credit Price = 2 TC Show Detailed Course Description. Overview. This course provides hardware designers with an overview of the capabilities and support for the Zynq® UltraScale+™ MPSoC family from a hardware architectural perspective. ...

Zynq UltraScale+ MPSoC Datasheet - Xilinx | DigiKey

The Zynq Ultrascale+ MPSoC development kit carrier board supports

the required set of features like FMC+ (HPC), FMC (HPC), FireFly, QSFP, SFP+, 12-Pin Pmod, and HDMI- IN/OUT connectors to validate Zynq Ultrascale+ MPSoC high-speed PL interfaces and PCIe x4, SATA, USB-Type-C, Display Port, Gigabit Ethernet and SDI Video IN/OUT on-board connectors to validate the Zynq Ultrascale+ MPSoC high-speed PS interfaces.

Zynq UltraScale+ MPSoC Base Targeted Reference Design

Zynq UltraScale+ MPSoCs Multiprocessors - Xilinx | Mouser

The Zynq® UltraScale+™ MPSoC family is based on the Xilinx® UltraScale™ MPSoC architecture. This family of products integrates a feature-rich 64-bit quad-core or dual-core Arm® Cortex™ - A53 and dual-core Arm Cortex-R5 based

processing system (PS) and Xilinx programmable logic (PL) UltraScale architecture in a single device.

UltraScale MPSoC Architecture - Xilinx

Zynq® UltraScale+™ MPSoC devices provide 64-bit processor scalability while combining real-time control with soft and hard engines for graphics, video, waveform, and packet processing.

Automotive Grade Zynq UltraScale+ MPSoCs

The MPSoC supports Quad/Dual Cortex A53 up to 1.5GHz with programmable logic cells ranging from 192K to 504K. The SOM supports high-speed connectivity peripherals such as PCIe, USB3.0, SATA3.1, Display port, Gigabit Ethernet through GTR high-speed transceivers from MPSoC. Mouse over

the image for zoom

*Zynq UltraScale+ MPSoC Data Sheet:
Overview (DS891)*

The Zynq® UltraScale+™ MPSoC Processing System wrapper instantiates the processing system section of the Zynq UltraScale+ MPSoC for the programmable logic and external board logic. The wrapper includes unaltered connectivity and some logic functions for some signals.

The Xilinx Automotive XA Zynq® UltraScale+™ MPSoC family is qualified according to AEC-Q100 test specifications with full ISO26262 ASIL-C level certification. The product integrates a feature-rich 64-bit quad-core ARM® Cortex™-A53 and dual-core ARM Cortex-R5 based processing system (PS) and Xilinx programmable logic (PL) UltraScale architecture in a single device.