Cmos Test And Evaluation A Physical Perspective

Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits
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CMOS VLSI
Microelectronic Test Structures for CMOS Technology
Automatic Testing and Evaluation of Digital Integrated Circuits
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Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits
Springer Science & Business Media
Piezoresistive stress sensing chips have been used extensively for measurement of assembly related die surface stresses. Although many experiments can be performed with resistive structures which are directly bonded, for extensive stress mapping it is necessary to have a large number of sensor cells which can be addressed using CMOS logic circuitry. Our previous test chip, the ATC04, has 100 cells, each approximately 0.012 in. on a side, on a chip with a side dimension of 0.45 in. When a cell resistor is addressed, it is connected to a four terminal measurement bus through CMOS transmission gates. In theory, the gate resistances do not affect the measurement. In practice, there may be subtle effects which appear when very high accuracy is required. At high temperatures, gate leakage can increase to a point at which the resistor measurement becomes inaccurate. For ATC04 this occurred at or above 50 C. Here, we report on the first measurements obtained with a new prototype test chip, the ATC06. This prototype was fabricated in a 0.5 micron feature size silicided CMOS process using the MOSIS prototyping facility. The cell size was approximately 0.004 in. on a side. In order to achieve piezoresistive behavior for the implanted resistors it was necessary to employ a non-standard silicide ''blocking'' process.

The stress sensitivity of both implanted and polysilicon blocked resistors is discussed. Using a new design strategy for the CMOS logic, it was possible to achieve a design in which only 5 signals had to be routed to a cell for addressing vs. 9 for ATC04. With our new design, the resistor under test is more effectively electrically isolated from other resistors on the chip, thereby improving high temperature performance. We present data showing operation up to 140 C.

CMOS Circuit Design and Test Patterns for Built-in Overcurrent Testing Springer Science & Business Media

Power supply current monitoring to detect CMOS IC defects during production testing quietly laid down its roots in the mid-1970s. Both Sandia Labs and RCA in the United States and Philips Labs in the Netherlands practiced this procedure on their CMOS ICs. At that time, this practice stemmed simply from an intuitive sense that CMOS ICs showing abnormal quiescent power supply current (IDDQ) contained defects. Later, this intuition was supported by data and analysis in the 1980s by Levi (RACD, Malaiya and Su (SUNY-Binghamton), Soden and Hawkins (Sandia Labs and the University of New Mexico), Jacomino and co-workers (Laboratoire d'Automatique de Grenoble), and Maly and co-workers (Carnegie Mellon University). Interest in IDDQ testing has advanced beyond the data reported in the 1980s and is now focused on applications and evaluations involving larger volumes of ICs that improve quality beyond what can be achieved by previous conventional means. In the conventional style of testing one attempts to propagate the logic states of the suspended nodes to primary outputs. This is done for all or most nodes of the circuit. For sequential circuits, in particular, the complexity of finding suitable tests is very high. In comparison, the IDDQ test does not observe the logic states, but measures the integrated current that leaks through all gates. In other words, it is like measuring a patient's temperature to determine the state of health. Despite perceived advantages, during the years that followed its initial announcements, skepticism about the practicality of IDDQ testing prevailed. The idea, however, provided a great opportunity to researchers. New results on test generation, fault simulation, design for testability, built-in self-test, and diagnosis for this style of testing have since been reported. After a decade of research, we are definitely closer to practice.

Testing of Digital CMOS Integrated Circuits Springer Science & Business Media

Device testing represents the single largest manufacturing expense in the semiconductor industry, costing over $40 billion a year. The most comprehensive and wide ranging book of its kind, Testing of Digital Systems covers everything you need to know about this vitally important subject. Starting right from the basics, the authors take the reader through automatic test pattern generation, design for testability and built-in self-test of digital circuits before moving on to more advanced topics such as IDDQ testing, functional testing, delay fault testing, memory testing, and fault diagnosis. The book includes detailed treatment of the latest techniques including test generation for various fault models, discussion of testing techniques at different levels of integrated circuit hierarchy and a chapter on system-on-a-chip test synthesis. Written for students and engineers, it is

both an excellent senior/graduate level textbook and a valuable reference.
CMOS/SOS Test Patterns for Process Evaluation and Control CRC Press
Defect oriented testing is expected to play a significant role in coming generations of technology. Smaller feature sizes and larger die sizes will make ICs more sensitive to defects that can not be modeled by traditional fault modeling approaches. Furthermore, with increased level of integration, an IC may contain diverse building blocks. Such blocks include, digital logic, PLAs, volatile and non-volatile memories, and analog interfaces. For such diverse building blocks, traditional fault modeling and test approaches will become increasingly inadequate. Defect oriented testing methods have come a long way from a mere interesting academic exercise to a hard industrial reality. Many factors have contributed to its industrial acceptance. Traditional approaches of testing modern integrated circuits (ICs) have been found to be inadequate in terms of quality and economics of test. In a globally competitive semiconductor market place, overall product quality and economics have become very important objectives. In addition, electronic systems are becoming increasingly complex and demand components of highest possible quality. Testing, in general and, defect oriented testing, in particular, help in realizing these objectives. Defect Oriented Testing for CMOS Analog and Digital Circuits is the first book to provide a complete overview of the subject. It is essential reading for all design and test professionals as well as researchers and students working in the field. `A strength of this book is its breadth. Types of designs considered include analog and digital circuits, programmable logic arrays, and memories. Having a fault model does not automatically provide a test. Sometimes, design for testability hardware is necessary. Many design for testability ideas, supported by experimental evidence, are included.' ... from the Foreword by Vishwani D. Agrawal
Evaluation of Dynamic Current Testing for CMOS Domino Circuits Cambridge University Press
Using the book and the software provided with it, the reader can build his/her own tester arrangement to investigate key aspects of analog-, digital- and mixed system circuits Plan of attack based on traditional testing, circuit design and circuit manufacture allows the reader to appreciate a testing regime from the point of view of all the participating interests Worked examples based on theoretical bookwork, practical experimentation and simulation exercises teach the reader how to test circuits thoroughly and effectively
Testing of Digital Systems Artech House Publishers
Transient current (iDDT) refers to the current drawn from the power supply durin g the transient switching of CMOS gates. Testing based on the transient current can detect many of the defects that can occur in ICs, such as resistive opens, w hich may not be detected by traditional voltage testing or by Leakage current (I DDQ) testing methods. A major set back for IDDQ testing methods is the increased leakage currents in today's ICs. Thus iDDT based testing has been often investi gated as an alternative or supplement to (IDDQ) testing. Little work has focused on iDDT testing for domino circuits. In this thesis, we propose a method for testing domino CMOS circuits using the transient power

supp ly current. The method is based on monitoring the peak value of the transient cu rrent. This peak varies considerably with process variations, so each process ha s different thresholds; this problem will be addressed by proposing a normalizat ion procedure that allows us to use a single threshold for all processes. We pre sent also a test vector generation algorithm for testing large domino circuits. We evaluate the effectiveness of this testing method by simulation on various do mino circuits of different sizes. We develop and implement a partitioning technique to improve the fault coverage of the test method when used with large circuits. The algorithm divides the circ uit into different clusters where each cluster is fed by a different power suppl y branch. We also provide an automation system to simplify the process of genera ting the simulation files, injecting the defects in the circuit, running the sim ulations, storing the simulations output, processing the output signals, and fin ally gathering and analyzing the results.

Design and Experimental Evaluation of a 3rd Generation Addressable CMOS Piezoresistive Stress Sensing Test Chip Springer

The 2nd edition of defect oriented testing has been extensively updated. New chapters on Functional, Parametric Defect Models and Inductive fault Analysis and Yield Engineering have been added to provide a link between defect sources and yield. The chapter on RAM testing has been updated with focus on parametric and SRAM stability testing. Similarly, newer material has been incorporated in digital fault modeling and analog testing chapters. The strength of Defect Oriented Testing for nano-Metric CMOS VLSIs lies in its industrial relevance.

CMOS Electronics Springer Science & Business Media

The definition from SEMATECH of wafer level reliability test is: a methodology to assess the reliability impact of tools and processes by testing mechanism-specific test structures under accelerated conditions during device processing. Because wafer level reliability test is the accelerated test, it owns some different characters with common long time test in terms of failure mechanisms, test procedures, life time prediction, test structures design and so on. In this book, all items of wafer level reliability of CMOS devices and processes will be discussed. The purpose of this book is to provide a good and urgently need reference on MOS device reliability. The authors discuss how to enhance the veracity of lifetime prediction and the effects to degrade the veracity deeply. Finally, a discussion of the problems with wafer level reliability in terms of the engineering applications and research is given.

Testing and Reliable Design of CMOS Circuits Springer Science & Business Media

Abstract: "In this paper we propose a very-low-voltage testing technique for CMOS logic IC's. Voltage dependence of CMOS logic circuit operation in the presence of resistive shorts and hot carrier damage is studied. It is shown that at certain much-lower-than-normal power supply voltage, weak CMOS logic IC's due to the presence of these flaws can be forced to malfunction while truly good IC's continue to function. Very- low-voltage testing also detects pattern dependent faults caused by resistive shorts. Because of its simplicity and because there is no overhead associated with it, very-low-

voltage testing can easily be applied to chips and circuit boards as a production test, field test, or failure diagnosis technique."

Test Generation and Evaluation for Bridging Faults in CMOS VLSI Circuits
Springer
The 2nd edition of defect oriented testing has been extensively updated. New chapters on Functional, Parametric Defect Models and Inductive fault Analysis and Yield Engineering have been added to provide a link between defect sources and yield. The chapter on RAM testing has been updated with focus on parametric and SRAM stability testing. Similarly, newer material has been incorporated in digital fault modeling and analog testing chapters. The strength of Defect Oriented Testing for nano-Metric CMOS VLSIs lies in its industrial relevance.

Gamma Irradiation Testing of Electronic Devices, and Evaluation of Irradiated CMOS Components on MOSIS Test Chips
Springer
CMOS Test and Evaluation: A Physical Perspective is a single source for an integrated view of test and data analysis methodology for CMOS products, covering circuit sensitivities to MOSFET characteristics, impact of silicon technology process variability, applications of embedded test structures and sensors, product yield, and reliability over the lifetime of the product. This book also covers statistical data analysis and visualization techniques, test equipment and CMOS product specifications, and examines product behavior over its full voltage, temperature and frequency range.

CMOS Life Suitability Evaluation Program
John Wiley & Sons
A reliability evaluation of Complementary Metal Oxide Semiconductor (CMOS) microcircuits which were made hard to total ionizing dose by means of ion implanting aluminum in the gate insulator was conducted. The testing revealed the existence of room temperature threshold voltage instabilities. Failure analysis isolated the cause to charge migration within the insulator. A complete description of the instability in relation to temperature and gate voltage is developed. Finally, a model for the CMOS behavior under temperature bias conditions as well as radiation response is proposed. (Author).

CMOS Test and Evaluation Springer Science & Business Media
The results of a matrix of high-temperature accelerated life tests, 125C life tests, and 250 hour 250C lot acceptance tests were evaluated to determine the reliabiltiy of a cross-section of the complementary metal oxide semiconductor (CMOS) family of devices. The devices evaluated included a NOR gate, a flip-flop, a four bit adder, and a counter/divider. Each device was procured from two different manufacturers, and from three different lots of each manufacturer. The correlation of the Lot Acceptance data with the reliability of the devices revealed that the Class S Lot Acceptance Test, as specified in MIL-STD-883, Method 500.5 is approximately 50% effective screening for lot reliability. To minimize the possibility of rejecting good lots and/or accepting bad lots, two temperature Lot Acceptance Test is recommended. Using a two temperature Lot Acceptance Test at temperature above 200 C would permit control of both the activation energy and pre-exponential factor in the Arrhenius model. A 100%

burn-9n is also recommended. Although burn-in would not improve all lots, it would improve the reliability of those lots which have a freak population with a high failure rate.

The Design, Testing, and Analysis of a Comprehensive Test Pattern for Measuring CMOS/SOS Process Performance and Control

The IC test industry has struggled for more than 30 years to establish a test approach that would guarantee a low defect level to the customer. We propose a comprehensive strategy for testing CMOS ICs that uses defect classes based on measured defect electrical properties. Defect classes differ from traditional fault models. Our defect class approach requires that the test strategy match the defect electrical properties, while fault models require that IC defects match the fault definition. We use data from Sandia Labs failure analysis and test facilities and from public literature. We describe test pattern requirements for each defect class and propose a test paradigm.

Reliability Evaluation of Aluminum Implanted CMOS Microcircuits

This book discusses in detail the correlation between physical defects and logic faults, and shows you how Iddq testing locates these defects. The book provides planning guidelines and optimization methods and is illustrated with numerous examples ranging from simple circuits to extensive case studies.

Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits

Advances in design methods and process technologies have resulted in a continuous increase in the complexity of integrated circuits (ICs). However, the increased complexity and nanometer-size features of modern ICs make them susceptible to manufacturing defects, as well as performance and quality issues. Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits covers common problems in areas such as process variations, power supply noise, crosstalk, resistive opens/bridges, and design-for-manufacturing (DfM)-related rule violations. The book also addresses testing for small-delay defects (SDDs), which can cause immediate timing failures on both critical and non-critical paths in the circuit. Overviews semiconductor industry test challenges and the need for SDD testing, including basic concepts and introductory material Describes algorithmic solutions incorporated in commercial tools from Mentor Graphics Reviews SDD testing based on "alternative methods" that explores new metrics, top-off ATPG, and circuit topology-based solutions Highlights the advantages and disadvantages of a diverse set of metrics, and identifies scope for improvement Written from the triple viewpoint of university researchers, EDA tool developers, and chip designers and tool users, this book is the first of its kind to address all aspects of SDD testing from such a diverse perspective. The book is designed as a one-stop reference for current industrial practices, research challenges in the domain of SDD testing, and recent developments in SDD solutions.

Testing a CMOS Operational Amplifier Circuit Using a Combination of Oscillation and IDDQ Test Methods

The CMOS D-latch is an important block in the design of sequential circuits. Thus, a new fully testable CMOS D-latch (FTD) is proposed. A comprehensive test set that includes possible physical failures is

developed. This test set is then applied to the FTD. The cost of implementation, analysis, and simulation of the FTD are all presented. Application of the FTD-latch to build a polarity-hold shift register is shown.

Design, Testing and Analysis of Test Patterns for CMOS Process Control and Monitoring

Microelectronic Test Structures for CMOS Technology and Products addresses the basic concepts of the design of test structures for incorporation within test-vehicles, scribe-lines, and CMOS products. The role of test structures in the development and monitoring of CMOS technologies and products has become ever more important with the increased cost and complexity of development and manufacturing. In this timely volume, IBM scientists Manjul Bhushan and Mark Ketchen emphasize high speed characterization techniques for digital CMOS circuit applications and bridging between circuit performance and characteristics of MOSFETs and other circuit elements. Detailed examples are presented throughout, many of which are equally applicable to other microelectronic technologies as well. The authors' overarching goal is to provide students and technology practitioners alike a practical guide to the disciplined design and use of test structures that give unambiguous information on the parametrics and performance of digital CMOS technology.

Defect Oriented Testing for CMOS Analog and Digital Circuits

An efficient automatic test pattern generator for I$sb{DDQ}$ current testing of CMOS digital circuits is presented. The complete two-line bridging fault set is considered. Because of the time constraints of I$sb{DDQ}$ testing, an adaptive genetic algorithm (GA) is used to generate compact test sets. To accurately evaluate the test sets, fault grading is performed using a switch-level fault simulator and a mixed-mode electrical-level fault simulator. The test sets are compared with those generated by HITEC, a traditional gate-level test generator. Experimental results for ISCAS85 and ISCAS89 benchmark circuits are presented. The results show that for I$sb{DDQ}$ testing, the GA test sets outperform the HITEC test sets. When the test sets are truncated due to test time constraints, the fault coverages can differ by 10% or more. In addition to test generation and test evaluation, diagnosis (fault location) is also performed using both test sets. Diagnosis is performed using fault dictionaries constructed during test evaluation. In addition to the traditional full dictionary, two reduced dictionaries are also presented. The results show that the reduced dictionaries offer good size-resolution trade-offs when compared with the full dictionary.

CMOS/SOS Test Patterns for Process Evaluation and Control

CMOS manufacturing environments are surrounded with symptoms that can indicate serious test, design, or reliability problems, which, in turn, can affect the financial as well as the engineering bottom line. This book educates readers, including non-engineers involved in CMOS manufacture, to identify and remedy these causes. This book instills the electronic knowledge that affects not just design but other important areas of manufacturing such as test, reliability, failure analysis, yield-quality issues, and problems. Designed specifically for the many non-

electronic engineers employed in the semiconductor industry who need to reliably manufacture chips at a high rate in large quantities, this is a practical guide to how CMOS electronics work, how failures occur, and how to diagnose and avoid them. Key features: Builds a grasp of the basic electronics of CMOS integrated circuits and then leads the reader further to understand the mechanisms of failure. Unique descriptions of circuit failure mechanisms, some found previously only in research papers and others new to this publication. Targeted to the CMOS industry (or students headed there) and not a generic introduction to the broader field of electronics. Examples, exercises, and problems are provided to support the self-instruction of the reader.